Page 2, replace the paragraph beginning on line 8, as follows:

As shown in Fig. 5A, on a semiconductor substrate 21, an element separating insulating film 22, a first interlayer insulating film 23, the first contact plug 24, a second interlayer insulating film 25, and the second contact plug 26 are arranged.

Page 3, replace the paragraph beginning on line 15, as follows:

Another example of the method shown in Fig. 5C using the contact plug is a conventionally known memory cell, that is, DRAM (Dynamic Random Access Memory) having a contact plug. An example of the cross-sectional structure of this type of memory cell is explained with reference to Fig. 6. In this structure, wiring for calling signals, which is called a bit line or a signal line, is formed under the layer lower than the charge accumulation capacitor 60.

Page 3, replace the paragraph beginning on line 25, as follows:

--A first interlayer insulating film 56 is formed so as to cover the element separating film 52 and the MOSFET. In order to connect the source-drain regions 51 and the first wiring layer formed on the first interlayer insulating

film 56, polysilicon plugs 54 and 55 are formed. The bit wiring 57 on the first interlayer insulating film 56 is made of tungsten silicide. A second interlayer insulating film 58 is formed so as to cover the bit wiring. A bottom electrode 59 of the capacitor is formed on the second interlayer, a capacitor dielectric film 60 is formed so as to cover the bottom electrode 59, and the upper layer of the capacitor dielectric film 60 is an upper electrode 61. The bottom electrode 59, the capacitor dielectric film 60, and the upper electrode 61 constitute a charge accumulation capacitor.--

Page 8, replace the paragraph beginning on line 1, as follows:

Figs. 2A to 2C are cross-sectional views showing the manufacturing process for a semiconductor device according to the first embodiment of the present invention.

Page 8, replace the paragraph beginning on line 3, as follows:

Figs. 3A to 3C are cross-sectional views showing the manufacturing process for a semiconductor device according to the first embodiment of the present invention.

Page 8, replace the paragraph beginning on line 5, as follows:

Fig. 4 is a cross-sectional view of a semiconductor device according to the second embodiment of the present invention.

Page 9, replace the paragraph beginning on line 21, as follows:

Since the silicide pad 5, formed on the upper end surface of polysilicon plug 4, is disposed in a self-aligning manner, the silicide pad 5 is aligned on the polysilicon plug and there is room to align the silicide pad on the tungsten plug 7, so that the connection between the silicide pad and the polysilicon plug 4 and the tungsten plug 7 can be secured without concern for failure in connection.

Page 12, replace the paragraph beginning on line 23, as follows:

Subsequently, a BPSG film is formed at a thickness of 500 nm as the second interlayer insulating film 20 on the above formed films. The second contact hole is opened through the second interlayer insulating film 20 by conventionally known photolithography and the dry-etching process. A titanium nitride film is formed by spattering as a barrier layer between the adhered layer and silicon for